



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

N

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,765	09/10/2003	Yukiya Hirabayashi	116801	4078
25944	7590	12/14/2004	EXAMINER	
OLIFF & BERRIDGE, PLC				SCHECHTER, ANDREW M
P.O. BOX 19928				
ALEXANDRIA, VA 22320				
ART UNIT		PAPER NUMBER		
		2871		

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,765	HIRABAYASHI, YUKIYA	
	Examiner Andrew Schechter	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 February 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 10 September 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/10/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Electro-optical device where common electrode does not overlap peripheral driving circuit, method of making same, and electronic apparatus".

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
3. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the construction "a portion, where the common electrode overlaps with the peripheral driving circuit or with wiring lines ... being removed" is potentially unclear. Does this mean it can be removed from over one but not necessarily both, or it must be removed from over both? For examining purposes, it is assumed that it must be removed from over both. There are similar constructions in claims 2 and 6, and claims 3-5 and 7 depend from claim 1.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by *Young*, U.S. Patent No. 6,246,460.

Young discloses [see Figs. 1 and 2] an electro-optical device comprising an active matrix substrate [25] having on the same plane a plurality of scanning lines [14], a plurality of signal lines [16] provided to intersect the scanning lines, a plurality of pixel electrodes [18] provided at the intersection portions of the scanning and signal lines, and a peripheral driving circuit [44 or 30] to matrix drive the pixel electrodes; a counter substrate [26], one surface thereof being provided with a common electrode [32] over the entire surface thereof, facing the active matrix substrate such that the common electrode is opposite to the pixel electrodes; and a liquid crystal layer [24] interposed between the active matrix substrate and the counter substrates; the counter substrate being provided so as to not overlap with the peripheral driving circuit or with wiring lines [such as 40, 41] to supply signals to the peripheral driving circuit in plan view. Claim 2 is therefore anticipated.

6. Claims 1, 5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by *Sawatsubashi et al.*, U.S. Patent No. 5,148,301.

Sawatsubashi discloses [see Figs. 3-5] an electro-optical device comprising an active matrix substrate [101] having on the same plane a plurality of scanning lines [G1-Gm], a plurality of signal lines [D1-Dn] provided to intersect the scanning lines, a plurality of pixel electrodes [103] provided at the intersection portions of the scanning and signal lines, and a peripheral driving circuit [112, 113] to matrix drive the pixel electrodes; a counter substrate [102] having a common electrode [105] on one surface and facing the active matrix substrate such that the common electrode is opposite to the pixel electrodes; and a liquid crystal layer [109] interposed between the active matrix substrate and the counter substrates; a portion, where the common electrode overlaps with the peripheral driving circuit or with wiring lines [114] to supply signals to the peripheral driving circuit in plan view, being removed [see Figs. 3 and 4]. Claim 1 is therefore anticipated.

The peripheral driving circuit includes a data line driving circuit [112], and the wiring lines include clock signal lines and image signal lines [col. 5, lines 33-38], so claim 5 is also anticipated. This is an electronic apparatus, so claim 7 is also anticipated.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.*, U.S. Patent No. 5,148,301 as applied to claim 1 above, and further in view of *Segawa*, U.S. Patent No. 5,506,707, *Yamamoto et al.*, U.S. Patent No. 5,657,100, and *Kubota et al.*, U.S. Patent No. 6,355,314.

Sawatsubashi discloses a method of manufacturing an electro-optical device, comprising forming a plurality of pixel electrodes [103] and a peripheral driving circuit [112, 113] to matrix drive the plurality of pixel electrodes on one surface of an active matrix substrate [101]; forming a common electrode [105] on one surface of a counter substrate [102] which does not overlap with the peripheral driving circuit or with wiring lines [114] for supplying signals to the peripheral driving circuit in plan view; bonding the active matrix substrate to the counter substrate with a predetermined gap therebetween using a sealing material [108] such that the common electrode is opposite to the pixel electrodes; and forming a liquid crystal layer by injecting liquid crystal into a space formed by the active matrix substrate, the counter substrate, and the sealing material [col. 4, lines 40-42].

Sawatsubashi does not explicitly disclose forming the common electrode over the entire surface of the counter substrate and then removing the recited portion.

Sawatsubashi forms the same structure, but is silent on the method used to pattern the common electrode. There are two ways it could be done: 1) the recited technique, covering the entire counter substrate with the common electrode, and then removing the recited portion, or 2) using a deposition mask so that the material for the common electrode is only deposited in the desired regions, so nothing has to be removed.

Segawa discloses making a counter electrode using the first technique, first sputtering ITO then etching it [col. 5, lines 10-29]. *Yamamoto* discloses making a counter electrode using the first technique, first sputtering and then etching [col. 4, lines 16-21]. *Kubota* discloses making a counter electrode using the first technique, first vacuum depositing the material then etching it [col. 37, lines 11-15]. It would have been obvious to one of ordinary skill in the art at the time of the invention to do it this way, motivated by the conventional nature of this technique (as evidenced by these references) which results in benefits to manufacturing time and cost from using existing production methods. Claim 6 is therefore unpatentable.

9. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.*, U.S. Patent No. 5,148,301 as applied to claim 1 above, and further in view of *Yamamoto et al.*, U.S. Patent No. 5,506,705.

Sawatsubashi does not disclose single crystal silicon TFTs or driving signals to the peripheral driving circuit at a frequency equal to or more than 10 MHz. For an analogous LCD, *Yamamoto* discloses using single crystal silicon TFTs and a driving signal of 10 MHz [col. 12, lines 1-25]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use single crystal silicon TFTs and a 10 MHz driving frequency in the device of *Sawatsubashi*, motivated by *Yamamoto's* teaching that this allows high speed driving and thus improves the display quality. Claims 3 and 4 are therefore unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Schechter
Andrew Schechter
Patent Examiner
Technology Center 2800
6 December 2004